COURSE DESCRIPTION CARD - SYLLABUS

Course name
Testing of digital systems

Course

Field of study
Electronics and Telecommunications
Area of study (specialization)

Level of study
Second-cycle studies
Form of study
full-time

Year/Semester
II/ Sem. 4
Profile of study
general academic
Course offered in
English
Requirements
elective

Number of hours

Lecture
30
Laboratory classes
15
Other (e.g. online)

Tutorials
0
Projects/seminars
0

Number of credit points
4

Lecturers

Responsible for the course/lecturer:
dr inż. Olgierd Stankiewicz,
olgierd.stankiewicz@put.poznan.pl

Responsible for the course/lecturer:

Prerequisites

Has basic knowledge of development trends in programmable systems.
Has sufficient knowledge to design specialized digital circuits for use in programmable systems.
Knows how basic communication interfaces work.
Knows the principles of designing basic elements of digital systems (state machines, pipelines).
Is able to obtain data from literature and other sources, he is able to integrate obtained information, interpret it, and formulate and justify opinions.
Can describe elements of a digital system in the form of Verilog language module.
Can test and verify the correct functioning of a digital system.
Can use learned design techniques to design a digital system.
Can use modern tools to support the design and synthesis of digital systems for the FPGA platform.
Is open to continuous learning opportunities and understands the need to improve his/her professional competence.
Has basic knowledge necessary to understand non-technical conditions of engineering activities; knows

the basic principles of occupational health and safety.
Has a sense of responsibility for designed electronic and telecommunication systems.

Course objective

To improve the student's knowledge and skills in the field:
- technology of protecting the digital system against permanent and temporary errors,
- fault detection and fault-tollerant systems,
- design verification methods,
- technologies for testing systems (BIST model).

Course-related learning outcomes

Knowledge

Knows how to test digital systems.
Knows how JTAG interfaces work.
Knows the principles of design/preparation of test modules.

Skills

Is able to obtain data from literature and other sources, he is able to integrate obtained information, interpret it, and formulate and justify opinions.
Is able to create a TestBench module for a digital system.
Is able to use modern tools for testing and verifying digital systems for the FPGA platform.

Social competences

Is open to continuous learning opportunities and understands the need to improve his/her professional competence.
Has basic knowledge necessary to understand non-technical conditions of engineering activities; he knows the basic principles of occupational health and safety.
Has a sense of responsibility for designed electronic and telecommunication systems.

Methods for verifying learning outcomes and assessment criteria

Learning outcomes presented above are verified as follows:
Lecture: written exam
The written exam is a set of 6-10 problematic questions, for which desciptory answer is expected.
Each answer is ranked from 0 to 1 points (fractinal points also possible).
The exam is passed if the number of attained points is greater than 50%. More than 50% indicates the knowledge above of satisfactory level.
The course issues of which the questions are prepared, are sent to students by e-mail using the university's e-mail system.

Laboratories:
Activity during classes, reports from particular activities. Laboratory project realized individually/in small groups.

Programme content

Test methods.
BIST model.
Compression of test and response vectors.
Methods of test data analysis.
Fault-Tolerant systems.
Verification of designs for FPGA systems.
Logical state analyzers for FPGA systems.

Teaching methods

Lecture: multimedia presentation with examples presented on the blackboard.

Laboratories: implementation of projects on computers (individual or in groups of few people). Examples illustrated on screen/blackboard.

Bibliography

Basic

Hajduk Z. Wprowadzenie do języka Verilog, BTC, Warszawa 2009.

Synthesis and Optimization of Digital Circuits / Synteza i optymalizacja układów cyfrowych, Giovanni De Micheli, WNT.
J.Rajski, J. Tyszer, Arithmetic Built-In Self-Test for Embedded Systems.

Additional

Łuba T. , Rawski M., Tomaszewicz P., Zbierzchowski B.: Synteza układów cyfrowych, Wydawnictwa Komunikacji i Łączności, Warszawa 2003.
Skahill K., VHDL Language / Język VHDL , WNT.
Kamionka-Mikuła H., Małysiak H., Pochopień B., Synteza i analiza układów cyfrowych, WKŁ.
Zbysiński P., Pasierbiński J.: Układy programowalne pierwsze kroki, Wydawnictwo BTC, Warszawa 2004.
Łuba T. Synteza układów logicznych. Oficyna Wyd. PW, Warszawa, 2005.

Breakdown of average student's workload

	Hours	ECTS
Total workload	100	4,0
Classes requiring direct contact with the teacher	58	2,0
Student's own work (literature studies and online tutorials, preparation for laboratory classes, preparation for exam) [1]	42	2,0

[1] delete or add other activities as appropriate